AMENDMENTS TO THE DRAWINGS

Please amend the drawings as described below. The "Annotated Mark-Up Drawing Sheet" shows the changes in red ink. The associated "Replacement Drawing Sheet" corresponds to the description of the amendments appearing below.

Please note that paragraph [0014] has been amended to correspond to amendments made to FIG. 1.

Attachments: Annotated Mark-Up Drawing Sheet

Replacement Drawing Sheet

<remainder of page intentionally left blank>

REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 1-16, 18-23 are pending in this application. Claims 15, 16, and 19 have been amended. Claims 17, 24 and 25 have been canceled.

DRAWINGS

In response to the Examiner's drawing objection, Applicants have amended FIG. 1 to show features recited in claims 8 and 16. Support for the amendment to the drawing can be found on paragraph [0014]. Withdraw of this rejection is respectfully requested.

SPECIFICATION

In response to the Examiner's objections to the specification, paragraphs 18 and 20 are replaced.

The Examiner has objected to the sentence found on page 6, line 3. However, Applicants note that if the sentence is amended per the Examiner's suggestion, the sentence does not make sense. The specification discloses that at least one of the unit delay circuits 120, 130, 140, 150 may be an inverter circuit. Amending the specification to disclose that an odd number of the unit delay circuits 120, 130, 140, 150 may be an inverter circuit does not make sense, and in addition, may introduce new matter.

The Examiner has objected to the disclosure found on page 6, paragraph [0020]. Applicants have amended paragraph [0020] to disclose that "the first through fourth groups may be approximately 1N:2N:3N:5N."

In view of the amendments, Applicants request withdrawal of the Examiner's objections.

CLAIM OBJECTIONS

In response to the Examiner's objections to claims 16 and 19, these claims have been amended. Claims 24 and 25 have been canceled in response to the Examiner's objection thereto. Applicants request withdrawal of the Examiner's objections.

REJECTIONS UNDER 35 U.S.C. §112

Claims 16 and 19 are rejected under 35 U.S.C. §112, second paragraph.

In response to the Examiner's rejection under §112, second paragraph, for claim 16, Applicants have amended claim 15 to recite "test **signals**." Accordingly, claim 16 is now definite. Please note a similar amendment was made to claim 8.

Claim 19 has been amended to recite oscillation waveforms are measured **at** a plurality of pads, not that a plurality of pads is **used** to measure oscillation waveforms.

In view of the amendments to claims 16 and 19, Applicants request withdraw of the Examiner's rejection under § 112, second paragraph.

REJECTIONS UNDER 35 U.S.C. §102(b)

Claims 1-2, 5-9, 12-21 and 24 and 25 are rejected under §102(b) as being anticipated by Inoshita et at. (USP 6,477,115). Applicants traverse this rejection.

Without acquiescing to the Examiner's other rejection reasons, the Examiner alleges that Inoshita et al. teaches a plurality of pads, each pad arranged so that at least one output terminal of unit delay circuits of the plurality of circuit groups is connected to each of the pads, respectively. For evidence, the Examiner alleges that reference sign "TAP1" is a pad. Applicants disagree.

As clearly disclosed in Inoshita et al. reference sign 7 relates to a pad, and reference sign "TAP1" relates intermediate data signal. Column 5, line 14, and column 11, line 51. Therefore, as illustrated in

FIGS. 1 and 14, each pad 7 **is not** arranged so that at least one output terminal of unit delay circuits of the plurality of circuit groups is connected to each of the pads.

The Examiner also alleges that Inoshita et al. also discloses "a different number of unit delay circuits. However, the section cited by the Examiner, column 15, lines 27-30, i.e., claim 2, recites different monitor circuits, each monitor circuit having a different delay circuit. "Different" used in claim 2 of Inoshita et al. means different type of delay circuit, for example, NAND, AND, OR gates. Column 10, lines 20-29. Therefore, Inoshita et al. does not suggest or teach different **number** of unit delay circuits.

Accordingly, for at least the reasons given above, independent claim 1, 8, and 15 are patentable over Inoshita et al. Dependent claims 2, 5-7, 9, 12-14, 16-21 are also in a condition for allowance for respectively depending on allowable independent claims.

REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 3-4, 10-11, and 22-23 are rejected under §103(a) as being unpatentable over Inoshita in view of Patrie et al. (USP 6,219,305).

As discussed with respect to the patentability of independent claims 1, 8, and 15, Inoshita fails to disclose all the features recited in independent claims 1, 8, and 15.

For at least the reasons given above, Applicants submit that dependent claims 3-4, 10-11 and 22-23 are patentable over Inoshita in view of Patrie et al. In addition, Patrie et al. fails to cure the deficiencies of Inoshita.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge any underpayment or non-payment of any fees required under 37 C.F.R. §§ 1.16 or 1.17, or credit any overpayment of such fees, to Deposit Account No. 08-0750, including, in particular, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C.

By: _____ Reg. No. 35,416

John A. Castellano, Reg. No. 35,094
P.O. Box 8910
Reston, VA 20195
(703) 668-8000

JAC/LYP/cm

FIG. 1